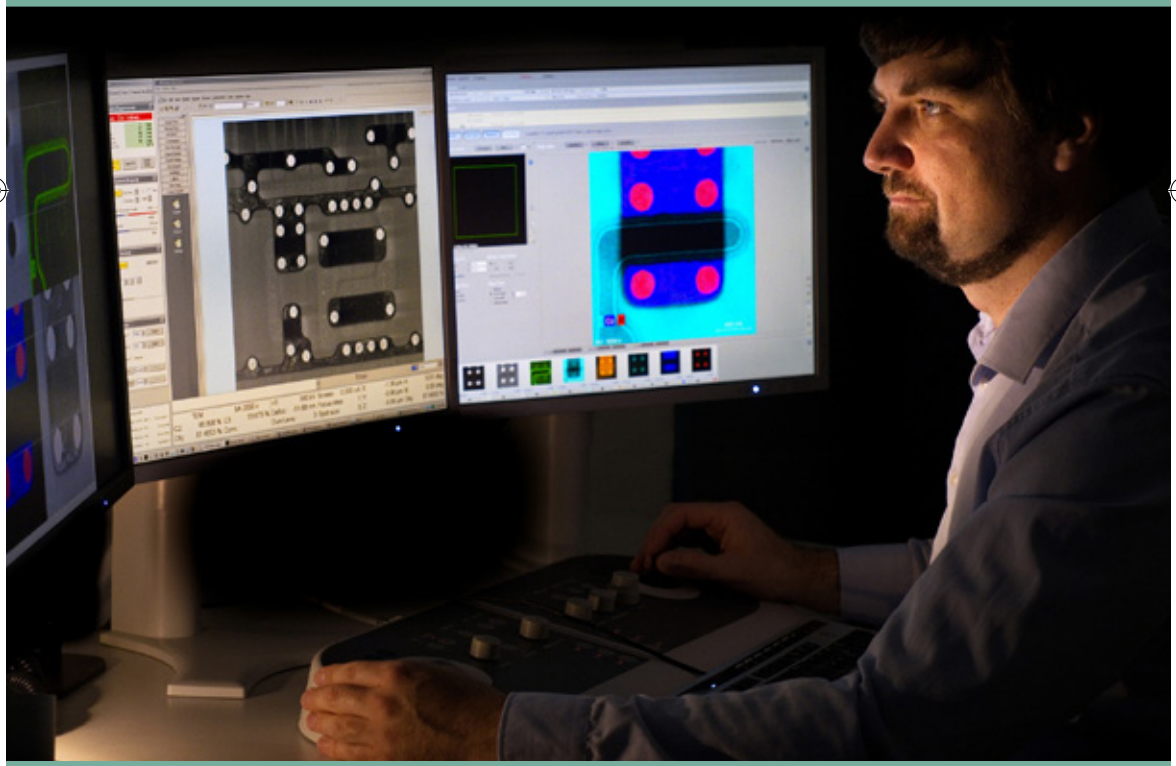
Fraunhofer IMWS

FRAUNHOFER INSTITUTE FOR MICROSTRUCTURE OF MATERIALS AND SYSTEMS IMWS

Innovation in Failure Analysis and Material Diagnostics of Electronics Components
11th CAM-Workshop 2024



Industry Workshop and Technology Exhibition

4th and 5th June 2024 I Halle (Saale) I Germany

Dear participants, partners and invited speakers,

As we gather for the latest edition of our workshop, it is with great pleasure that we embark on another insightful journey into the realms of failure analysis and material diagnostics in electronics. Over the years, the CAM Workshop has evolved into a cornerstone event for specialists and experts alike, providing a platform for robust discussions and knowledge exchange.

We are excited to bring you an impressive lineup of keynote presentations at CAM Workshop 2024, guaranteed to inform and motivate. Beginning our sessions, Frank Fournel from CEA-Leti in France will delve into the complexities of wafer-to-wafer and die-to-wafer direct bonding, pivotal for various 3D packaging applications. With his extensive experience in bonding technology engineering, Frank will examine the challenges and potentials of direct bonding techniques, offering invaluable insights into surface characterization, defect monitoring, and bonding interface analysis. Following this, Anton Chichkov from Chips Joint Undertaking in Belgium will introduce the EU Chips Act funding program, providing a glimpse into the regulatory landscape shaping semiconductor manufacturing in Europe. Then, Dr. Peter Friedrichs from Infineon Technologies AG in Germany will take a deep dive into SiC power devices and their robustness and reliability aspects, addressing the unique challenges and opportunities presented by the surge in demand for wide band gap-based solutions. Dr. Friedrichs will shed light on the intricate reliability assurance procedures and ruggedness aspects associated with SiC-based devices. Lastly, we will be joined by esteemed Prof. Dr. Zhiheng Huang from Sun Yat-sen University in China, who will explore the fascinating realm of applied microstructure for AI. Prof. Huang's expertise in materials science and engineering will unravel the intricate relationship between microstructure diagnostics, failure analyses, and artificial intelligence, demonstrating how microstructure hierarchy descriptors can revolutionize our understanding of materials at both electron and device levels, paving the way for innovative advancements in informatics and AI.

Once more, alongside the invited oral presentations, there will be an industrial exhibition featuring suppliers of failure analysis and material diagnostics equipment, facilitating direct interaction between electronics failure analysis experts and diagnostics equipment manufacturers. This hallmark concept has defined the CAM Workshop, establishing it as a globally recognized hub for discussion and networking in the field of failure diagnostics in electronics. We extend our heartfelt gratitude to our exhibitors and the international program committee for their unwavering support in ensuring the event remains an outstanding platform for collaboration and exchange.

One of the highlights of this year's workshop is the FA Technology Roadmap initiative. Led by ASM's Electronic Device Failure Analysis Society (EDFAS), this endeavor seeks to chart the course for future advancements in failure analysis methods and equipment. Last year, our esteemed panelists provided invaluable insights into the ongoing efforts of this initiative. Building upon that momentum, we now turn our attention to the responses of equipment providers to the industry-wide gap analysis survey. Their input will be instrumental in shaping the roadmap forward, ensuring that our industry remains at the forefront of innovation.

Get ready for two days filled with thrilling presentations and ample chances to network and socialize. Join us at the drinks reception in the exhibition area and at the networking dinner. We look forward to seeing you there!

On behalf of the program committee,
Frank Altmann

Content

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Ingrid De Wolf
IMEC (BELGIUM)

Ingrid De Wolf received the PhD in Physics from the KU Leuven, Belgium, in 1989. In the same year she joined IMEC, where she worked on microelectronics reliability, with special attention for mechanical stress analysis using micro-Raman spectroscopy and failure analysis. From 1999 to 2014, she headed the group REMO, where research is focused on reliability, test and modelling of 3D technology, interconnect, OIO, MEMS and packaging. She (co-)authored more than 550 publications. She is fellow at IMEC, IEEE senior member, professor at the Department of Materials Engineering of the KU Leuven and program director of the Master of Nanoscience, Nanotechnology and Nanoengineering at the Faculty of Engineering Science at the KU Leuven.

Joerg Krinke
ROBERT BOSCH GMBH (GERMANY)

Joerg Krinke received his Diploma in Materials Science from the Friedrich-Alexander- University of Erlangen-Nürnberg in 1995. Prior to joining Robert Bosch GmbH in 2000, he worked as a research associate where his work was mainly concerned with microstructural characterization and electrical behaviour of grain boundaries in polycrystalline Si by the means of EBIC and TEM. Since 2000, Joerg Krinke has worked as an engineer for reliability analyses of active electronic components, later becoming senior expert for reliability and technology assessment of first level packaging technologies of electronic components. Currently he is the Bosch project leader of the publicly sponsored project FA4.0 (Failure Analysis 4.0 – Key for reliable electronic devices in smart mobility and industrial production).

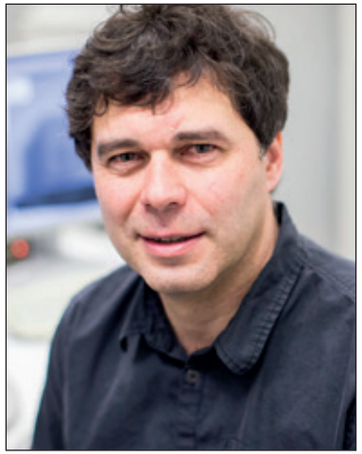
Frank Altmann
FRAUNHOFER IMWS (GERMANY)

Frank Altmann received his Diploma in Physics from the Technical University, Dresden. He joined the Fraunhofer IWM (now IMWS) in 1997 and has since been concerned with material diagnostics and failure analysis as well as with strength and reliability problems of semiconductor components. Since 2006 he has been head of the research group »Diagnostics of semiconductor technologies« with responsibility for national and international research projects with industry and public organizations focusing on Si and GaN chip technologies. Since 2019 he is acting head of the department »Electronic Materials and Components". Frank Altmann has authored and co-authored more than 60 publications and is active within several national and international failure analysis conference and education committees.

Pascal Gounet
STMICROELECTRONICS (FRANCE)

Pascal Gounet received his first diploma of engineering on microelectronics (ISTASE Institut Supérieur des Techniques Avancées Saint Etienne) in 1997. Then he went to the "Ecole des Mines" in Saint Etienne for a second diploma about software engineering received in 1998. He joined STMicroelectronics at the beginning of 1999 first as a designer (analog & digital circuits). He also worked in a CAD software development group. Since 2003, he is engineer in Failure Analysis. Elected in 2011 as physical & circuit edit analyzes expert, he currently works and develops on many topics like (but not limited to) sample preparation, SEM & FIB, microscopy, laser and plasma techniques and technologies.

Eckhard Langer
GLOBALFOUNDRIES INC (GERMANY)
REPRESENTING EUFANET



Eckhard Langer received his PhD in electrical engineering & micro systems technology from the Technical University of Chemnitz. He started his professional carrier at the Fraunhofer Institute of Mechanics of Materials Halle, where he worked in the field of microelectronics and materials analysis. In 1997 Eckhard Langer joined Advanced Micro Devices (AMD) in Dresden and until recently worked with GLOBALFOUNDRIES. As a director of the Central Lab Services he was responsible for the laboratories for material & physical failure analysis, reliability & electrical characterization and chemical analysis. He is currently working for Infineon Technologies AG and is a member of the EUFANET board.

Thomas Schweinboeck
INFINEON TECHNOLOGIES AG (GERMANY)

Thomas Schweinboeck received his PhD from University Regensburg (Experimental and Applied Physics, Micro- and Nanostructures). Since 2001, he has been working with Infineon Technologies, Munich, in the Central Failure Analysis Lab, performing electrical and physical analysis for all automotive products within Infineon, during this time also being responsible for method development projects dealing with Scanning Probe and Nano-probing topics. Since 2014, he has been leading a team for failure analysis of MEMS, sensor and bipolar/mixed signal devices. He has authored and co-authored several publications on FA method development and has acted as work package leader for EU funding projects SAM^3 and FA4.0.

Szu Huat Goh
QUALCOMM (SINGAPORE)

Szu Huat received his BEng and PhD in electrical and computer engineering from the National University of Singapore. He started his career with GLOBALFOUNDRIES, where he leads a team responsible for product failure diagnostics and advanced methodologies to accelerate yield ramp. He focuses on the development of wafer-level dynamic fault isolation techniques combining with cross-functional domain knowledge of design and test to enhance yield learning. His recent exploration centers on machine learning to enhance FA and yield prediction. He is currently with QUALCOMM yield management team where he is responsible for advanced technologies yield engineering and diagnostic. Szu Huat was the technical program chair, general co-chair and general chair for the International Physical and Failure Analysis (IPFA) in 2016, 2017 and 2018.

Tuesday, 4th June 2024

SESSION A: WELCOME AND KEYNOTES

09:00	**Welcome** Erica Lilleodden / Frank Altmann I Fraunhofer IMWS (DE)
09:20	**Keynote: Characterisation needs in wafer-to-wafer and die-to-wafer direct bonding** Frank Fournel I CEA-Leti (F)
10:00	**Keynote: EU Chips Act – An Introduction** Anton Chichkov I Chips Joint Undertaking (BE)
10:40	**Coffee Break / Exhibition**

SESSION B: HETEROGENEOUS INTEGRATION

11:20	**A Study of SiCN Wafer-to-Wafer Bonding and Impact of Wafer Warpage** Serena Iacovo I IMEC(BE)
11:40	**Assembly and Interconnection Technology with Nanowires** Sebastian Quednau I NanoWired (DE)
12:00	**Open Advanced Packaging / Micro Integration Foundry as a model for one manufacturing platform with integrated LAB-in-the-FAB concept** Torsten Grawunder I Swissbit Germany AG (DE)
12:20	**Approaches in high resolution non-destructive defect localization to meet current and future integration challenges** Sebastian Brand I Fraunhofer IMWS (DE)
12:40	**Robustness and reliability testing for heterointegration** Jan Proschwitz I Intel Deutschland GmbH (DE)
13:00	**Revolutionizing semiconductor testing: The power of automation in testing chiplets** Dirk Schade I XYZTec (DE)
13:20	**Lunch Break / Exhibition**

Tuesday, 4th June 2024

SESSION C: NOVEL FAILURE ANALYSIS TECHNIQUES

14:40	**Hybrid SIMS: New possibilities for advanced semiconductor structure analysis with Self-Focusing SIMS** Sven Kayser I IONTOF GmbH (DE)
15:00	**X-ray Assisted Device Alteration (XADA) for Future Generations of ICs with Backside Power Distribution Network** Wenbing Yun I Sigray, Inc. (US)
15:20	**Advances in EFA with Color Coded Multi-Channel Nanoprobing** Rene Hammer I Point Electronic GmbH (DE)
15:40	**Advancing the Quantification Workflow for 2D Charge Carrier Profiling by Scanning Spreading Resistance Microscopy** Thomas Adlmaier I Infineon Technologies Dresden GmbH (DE)
16:00	**FA methodologies for silicon photonics devices** Anjanashree Ramakrishna Sharma I IMEC and KU Leuven (BE)
16:20	**Coffee Break / Exhibition**

SESSION D: PANEL DISCUSSION

17:00	**Failure Analysis Roadmap Status & Vendor Feedback** Keith Serrels I NXP Semiconductors (US) Libor Strakoš I Thermo Fisher Scienitfic (CZ) Chris Richardson I Allied High Tech Products, Inc. (US) Martin Igarashi I TeraView LTD (UK) Lukáš Hladík I TESCAN GROUP, a.s. (CZ) Wenbing Yun I Sigray, Inc. (US) Thomas Rodgers I Carl Zeiss Research Microscopy GmbH (DE) Peter Hoffrogge I PVA TePla Analytical Systems GmbH (DE)
18:00	**Drinks Reception**
19:00	**Social Program: Networking Dinner**

Wednesday, 5th June 2024

SESSION E: TUTORIAL

08:00	**Machine Learning Based Data and Signal Analysis Methods for the Application in Failure Analysis** Michael Kögel I Fraunhofer IMWS (DE)
09:00	**Coffee Break / Exhibition**

SESSION F: SIC & GAN POWER ELECTRONICS

09:40	**Keynote: SiC power devices and related robustness and reliability aspects** Peter Friedrichs I Infineon Technologies AG (DE)
10:20	**Robustness for power electronic packaging** Thorsten Vehoff I Heraeus Electronics GmbH (DE)
10:40	**Gate-switching instability in silicon carbide power MOSFET's** Dick Scholten I Robert Bosch GmbH (DE)
11:00	**Integration of free-standing single crystal diamond (SCD) nanomembranes in ultra-wide bandgap electronics** Andreas Graff I Fraunhofer IMWS (DE)
11:20	**Power devices Failure Analysis Use Cases Using High voltage OBIRCh workflows** Antoine Reverdy I Sector Technologies (FR)

11:40	**Lunch Break / Exhibition**

Wednesday, 5th June 2024

SESSION G: FA WORKFLOWS AND DIGITALIZATION

13:00	**Keynote: Applied Microstructure for AI: From Electrons to Devices & From Diagnostics to Informatics** Prof. Dr. Zhiheng Huang I Sun Yat-sen University (CN)
13:40	**An Artificial Intelligence Powered Reconstruction and Metrology Workflow for Semiconductor Packaging Development using High-Resolution 3D X-ray Microscopy** Allen Gu I Carl Zeiss Research Microscopy Solutions (US)
14:00	**ML assisted defect detection for reliable failure analysis in microelectronic components** Amit Kumar Choudhary I Matworks GmbH (DE)
14:20	**In Depth Logic Analysis on Digital Designs** Fabian Rudau I Robert Bosch GmbH (DE)
14:40	**Integrated Workflows for Failure Analysis** Christian Hollerith I Infineon AG (DE)
15:00	**In-situ AFM-in-(FIB)SEM workflow for site-specific & correlative failure analysis of semiconductors** Libor Strakoš I Thermo Fisher Scientific (CZ)
15:20	**Automated SEM/EBIC Workflow for Wafer Level Failure Analysis** Oscar Recalde I Kleindiek Nanotechnik GmbH (DE)

4 Abstracts

Tues 09:20 - 10:00	**Keynote:** **Characterisation needs in wafer-to-wafer and die-to-wafer direct bonding**	Session A: Welcome and Keynotes

Frank Fournel I CEA-Leti I France

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Direct bonding is now a well-established technique that enables various 3D applications. Mass production of silicon dioxide to silicon dioxide bonding, as well as hybrid surfaces with copper pads, is in mass production within microelectronic foundries. However, hydrophilic direct bonding remains a challenging technology due to its very low adhesion energy, necessitating stringent control over surface properties such as flatness, roughness, and particle contamination. Before bonding, precise control of these surface parameters is mandatory.

Furthermore, post-bonding, it is imperative to monitor defectivity with a buried interface between 775µm of silicon. Bonding energy is also a crucial consideration, for which only destructive technology is currently available. Additionally, for in-depth analysis of the bonding interface, techniques such as X-ray, FTIR, or even neutron reflectivity are required.

While there are numerous failure analysis and surface material diagnostic methods at the wafer scale, the complexity significantly increases at the die scale, revealing vast challenges. As die-to-wafer bonding is on the verge of entering mass production, it is high time to extend the same characterization capabilities to this scale.

Frank Fournel, 48 years old, is a highly accomplished professional in the field of bonding technology engineering. n 2001, Frank Fournel obtained his PhD for his groundbreaking research conducted at CEA Grenoble. His work focused on utilizing molecular bonding to create twisted substrates, enabling the growth of self-positioning nanostructures. Following the completion of his doctoral studies, he joined CEA's thin film and circuit layers transfer laboratory, where he has made significant contributions.

Frank Fournel's primary area of expertise lies in the fundamental understanding of direct bonding and its practical applications in thin layer transfer techniques and substrate engineering. He has been actively involved in numerous international projects in collaboration with CEA's industrial partners. Currently, Frank serves as the head of bonding technology engineering at LETI.

Tues 11:20 - 11:40	**A Study of SiCN Wafer-to-Wafer Bonding and Impact of Wafer Warpage**	Session B: Heterogeneous Integration

Serena Iacovo I IMEC I Belgium

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Wafer to wafer bonding studies were carried out on blanket and patterned highly warped wafers using SiCN as bonding dielectric material to gain a deeper understanding of SiCN-to-SiCN direct bonding and to assess the impact of wafer shape on bonding overlay results. Regarding the fundamental understanding of SiCN bonding, characterization data show that the SiCN-to-SiCN interface is oxidized, suggesting strongly bonded due to the presence of covalent bonds, already at room temperature, in contrast to what has been hypothesized for SiO2 for which this reaction would start only by subjecting the bonded pair to an anneal of 150 °C. As concerns the impact of shapes on final bonding results, bonding experiments are carried out by combining different wafer shapes. Tools such as patterned wafer geometry (PWG) and a lithography scanner were used to measure the distortion signature of the wafers before and after bonding. Bonding recipe parameters were optimized to minimize overlay errors, on two different bonding tool configurations, for nominally flat wafers. The same parameters were used to bond the warped wafers to investigate the impact of wafer warpage.

Serena Iacovo received the B.Sc. and M.Sc. in electronic engineering from the University of Calabria, Italy, in 2008 and 2011 respectively. She obtained a PhD degree from the department of physics and astronomy, KU Leuven, Belgium in 2017. She joined imec in February 2017 and she is currently working as a senior R&D wafer bonding engineer working on most of the wafer-to-wafer permanent bonding activities at imec such as Hybrid, Backside PDN and 3D sequential integration. Her research is focusing on the physical mechanism behind direct bonding, void formation mechanisms and wafer-to-wafer overlay optimization. She has (co-)authored 20 research papers on room temperature wafer bonding.

Tues 11:40 - 12:00	**Assembly and Interconnection Technology with Nanowires**	Session B: Heterogeneous Integration

Sebastian Quednau I NanoWired I Germany

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NanoWired, founded in 2017 as a spin-off from TU Darmstadt, has developed and patented an interconnection technology known as the NanoWiring process. This process allows for the coating of various substrates with copper nanowires. From this foundation, several assembly processes have been derived: KlettWelding, KlettSintering, and KlettGlueing. The versatility of NanoWired's technologies enables the connection of electronics across a wide range of contact sizes – from several square centimeters for power electronic parts down to microelectronic parts with contact diameters as small as a few micrometers. Remarkably, even highly sensitive components can be connected due to the ability to work at very low temperatures, including room temperature. In this presentation, NanoWired will present the technology process flows and highlight its applications. Notably, the talk will delve into the use of NanoWired technology in GaN power electronics, exploring how flip chip technologies can enhance high-frequency behavior and reduce Rdson.

Sebastian completed his Diploma in Electrical Engineering at TU Darmstadt in 2010, specializing in Microelectromechanical Systems. He then pursued his PhD thesis at the same institution, focusing on the fabrication of metallic nanowires, which he successfully completed in 2015. Following this, Sebastian worked as a team leader in the field of Micro-Nano Integration at the Chair of MEMS Technology at TU Darmstadt.
In January 2017, he co-founded NanoWired GmbH, where he currently serves as the Chief Science Officer. NanoWired has garnered several awards and is poised to revolutionize industrial applications through its NanoWiring and related technologies.

Tues 12:00 - 12:20	**Open Advanced Packaging / Micro Integration Foundry as a model for one manufacturing platform with integrated LAB-in-the-FAB concept**	Session B: Heterogeneous Integration

Torsten Grawunder I Swissbit Germany AG I Germany

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The chip design process with Chiplets fundamentally changes the meaning and requirements of advanced packaging. Against the background that Swissbit Germany AG acts as a semiconductor backend manufacturer, the technological transformation process (SoC, SiP towards SoP) for advanced manufacturing is described, including the new meaning of Open Advanced Packaging / Micro Integration Foundry as a model for a manufacturing platform with integrated LAB-in-the-FAB concept. The diverse challenges that arise with the central idea of chiplets in relation to D2D bus systems, chiplet frameworks and its underlying design kits (CDK+ADK+WDK+SPDK) and the architectural designs in the chip packaging design process are described. The outstanding importance of integrating a LAB-in-the-FAB concept for a manufacturing platform for chiplets (SiP, SoP) will be presented.

Torsten Grawunder is a hardware / security engineer. He studied physics of electronic components with a specialization in ASIC design in the field of communication Technology at the Technical University of Chemnitz. Since 2021 he has been working at Swissbit Germany AG in system design / embedded solutions in the APATS department. Since then he has been creating / analyzing system concepts in pre-development for future NAND flash memory products and supervising the funding process of Swissbit. For over two decades, he has played a key role in the hardware development of encryption devices for ISDN, ATM and Ethernet in various companies (Biodata AG, secunet, Rohde & Schwarz SIT GmbH).

Tues 12:20 - 12:40	**Approaches in high resolution non-destructive defect localization to meet current and future integration challenges**	Session B: Heterogeneous Integration

Sebastian Brand I Fraunhofer IMWS I Germany

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Increasing miniaturization combined with steadily increasing complexity in interconnect technology and integration of new package and semiconductor materials highly challenges non-destructive inspection and quality assessment methods, necessary for defect reduction and reliability. General applicability of machine learning based data processing has been demonstrated and proven effective in various tasks related to the microelectronic failure analysis. However, to reach the next level of implementation into the everyday workflows and to obtain a broad acceptance development beyond the state of the art will be necessary. The paper describes the gap between existing solutions and the necessary requirements to decrease the operator's subjectivity and to increase the level of autonomy and automation for the application in high-resolution non-destructive defect detection and localization. Equipment related transfer characteristics in the acquired measurement data need to be removed for a generalized application and compatibility between different tools and to increase to degree of work-flow automation. Specific sample related features in the data will require specifically trained models and thus reduce the possible level of generalization. We will introduce novel concepts for removing specificities of the equipment and samples, concepts for deviation-based defect tracing as well as feast and efficient computing to allow for further automation of data and signal analysis in microelectronics failure identification and characterization.

Sebastian Brand is a senior scientist at the Fraunhofer IMWS, where he leads a research-, development and application team for non-destructive defect filocalization in the field of failure analysis and metrology. Sebastian holds a Ph.D. in electrical engineering which he received in 2004 from the University of Magdeburg, Germany. In 2004 and 2005 he joined the University of Toronto and Ryerson University in Toronto, Canada as a post-doctoral fellow working in fifithe field of cancer research.

Sebastian has 19 years of experience in the field of acoustics in life- and material sciences and authored /coauthored more than 60 fipublications in this and adjacent research fields. His current research extends from acoustic methods over Lock-In-Thermography to magnetic imaging where he and his team undertake research and development for non-destructive defect localization and characterization.

Tues 12:40 - 13:00	**Robustnes and reliability testing for heterointegration**	Session B: Heterogeneous Integration

Jan Proschwitz I Intel Deutschland GmbH I Germany

Heterogeneous integration of chiplets enables complex and compact electronic systems by breaking the limits of reticle size. This is achieved by combining function-optimized wafer technologies with manufacturing yield improvements. Over the past few years, different 2.XD and 3D packaging architectures have been developed and introduced for high performance compute applications as well as commercial products. However, the complexity of such advanced package constructions leads to new challenges for managing the intrinsic mechanical stress as well as for adapted electrical test strategies. The presentation will give an overview of these challenges and how robustness can be improved and how product validation can be implemented.

Jan Proschwitz is a Reliability Engineer at Intel Deutschland GmbH with over 20 years of experience in package and board level reliability in the semiconductor industry. In 2011 he joint Intel Deutschland GmbH. Jan Proschwitz studied electrical engineering at the Hochschule for Technik und Wirtschaft in Dresden, where he graduated as Dipl.-Ing (FH) in 1998.

Tues 13:00 - 13:20	**Revolutionizing semiconductor testing: The power of automation in testing chiplets**	Session B: Heterogeneous Integration

Dirk Schade I XYZTec I Germany

The rapid evolution of semiconductor technology has given rise to novel paradigms in chip design and manufacturing. Such innovation is the concept of chiplets, which involves breaking down a complex integrated circuit into smaller, interconnected components, each designed to perform specific functions. This article delves into the world of chiplets and their intrinsic connection to material testing. Chiplets offer numerous advantages, including enhanced flexibility, scalability, and cost-effectiveness in semiconductor design. However, the successful implementation of chiplets hinges on rigorous material testing and characterization to ensure reliability and performance. In conclusion, chiplets represent a transformative approach to semiconductor design, offering unparalleled opportunities for innovation and customization. However, the realization of their full potential relies heavily on robust material testing and characterization processes. This abstract underscores the critical relationship between chiplets and material testing, highlighting the challenges and advancements in this dynamic field that pave the way for the next generation of electronic devices.

Dirk Schade studied environmental technical and Business management (distance study) at the University of Applied Sciences in Merseburg. Since 1999 he has been actively involved in the semiconductor industry and started the management of XYZTEC Germany in 2002 and became additionally on international level "Global Sales Director". Furthermore, Mr. Schade is CEO of XYZTEC GmbH, American XYZTEC Incorporated, and a shareholder in several technology companies in the field of machinery and plant engineering. His focus is constantly on the growth of companies and the formation of networks. His special strengths are in the area of sales and marketing solutions particularly explanation-requiring products, connections to research communities, and procurement of venture capital.

Tues 14:40 - 15:00	**Hybrid SIMS: New possibilities for advanced semiconductor structure analysis with Self-Focusing SIMS**	Session C: Novel FA Techniques

Sven Kayser I IONTOF GmbH I Germany

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To boost the performances of the next generation transistors, new materials and device architectures have been investigated in the semiconductor industries. In this context, strained-Ge and SiGe channel FET's have received high interest.
As a consequence, characterization techniques have to provide chemical information and high sensitivity with a spatial resolution compatible with the device structure of down to 10 nm. Secondary Ion Mass Spectrometry (SIMS) provides excellent chemical information and low detection limits, but lacks the spatial resolution to directly probe devices from sub-10 nm technologies. Nevertheless, its applicability to analyze the composition of narrow trenches (< nm) has been enabled through the concept of Self-Focusing SIMS (SF-SIMS).
In this contribution, we will show that the improved mass resolution of the recently developed Hybrid SIMS instrument, using the Orbitrap™ mass analyzer in a SIMS instrument, is extremely beneficial for advanced semiconductor structure analysis.

Sven Kayser was born in Münster, Germany on 20th May 1969 and received the Diploma degree in Physics (within the department of surface science) from the University of Muenster in 1996. Since 1995 he was a member of the research group of Prof. Benninghoven. His work focused on the post ionization of sputter molecules using 193 nm pico-second laser pulses. In 1996 he joined the IONTOF company. Here he was initially responsible for the world-wide after sales service. At the beginning of 2004 he became the Sales and Marketing Manager of IONTOF.

Tues 15:00 - 15:20	**X-ray Assisted Device Alteration (XADA) for Future Generations of ICs with Backside Power Distribution Network**	Session C: Novel FA Techniques

Wenbing Yun I Sigray Inc. I USA

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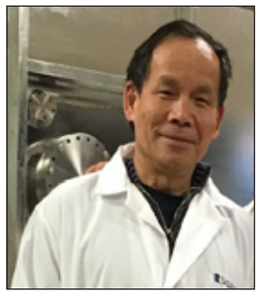
Backside power delivery (BPD) is widely anticipated by the semiconductor industry, enabling more efficient power delivery and significant improvements to transistor density. The challenge with BPD is that existing circuit debugging / fault isolation techniques such as LADA (laser assisted device alteration) will become obsolete. Because LADA requires backside silicon thinning, the shift to BPD in which power rails are placed on the backside means this approach will no longer work. One of the most promising approaches to address emerging BPD schemes. is using focused X-rays instead of NIR in a newly developed approach called X-ray Assisted Device Alteration (XADA). Because X-rays are sufficiently transmissive to Cu and Si, little to no sample preparation including backside thinning is required and the intact device can be probed. Recent work has demonstrated the effectiveness of using focused x-rays from a laboratory source for altering transistor threshold voltages (VT), changing ring oscillator (RO) frequencies and inducing timing shifts, including the localization of a physical defect using a real-world chip. Roadmap for smaller X-ray probe size to < 1 um will be discussed.



Dr. Wenbing Yun is a leading researcher in X-ray imaging, an innovator, a serial entrepreneur, and OSA fellow. He has over sixty issued patents on x-ray technology. Formerly a beamline scientist, he founded Xradia, Inc., a company aimed at enabling synchrotron-like x-ray microscopy in the laboratory. The company was successfully acquired by Carl ZEISS. Dr. Yun subsequently started Sigray, Inc. with a mission to make accessible all synchrotron analytical techniques to x-ray technologies by at least an order of magnitude. Sigray's growing product portfolio includes microXRF, XAS, and nano x-ray microscope systems, where key advantages lie in its patented x-ray source, optics and system designs

Tues 15:20 - 15:40	**Advances in EFA with Color Coded Multi-Channel Nanoprobing**	Session C: Novel FA Techniques

Rene Hammer I Point Electronic GmbH I Germany

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Key improvements to data acquisition, visualization and analysis are presented for Electrical Failure Analysis (EFA). Multi-channel image acquisition is introduced, where every nanoprobe is used for simultaneous imaging, in combination with color coding either by probe or by current. This new approach improves visualization of new device technologies with increasing three-dimensional complexity, in particular for overlapping structures and fields. Further, this new multichannel method opens opportunities for image mixing to improve data quality and signal interpretation.

Rene Hammer studied physics at Martin-Luther-University Halle-Wittenberg from 2002-2007 and obtained a diploma degree in 2007. From 2009-2015, he worked as a PhD student at the surface science group of the physics department at the same university. His research focused on the structural and electronic structure of thin organic films on noble-metal single-crystals using low-temperature scanning-tunneling microscopy and spectroscopy. He obtained his PhD degree in physics in 2015. From 2015-2016, he worked as a Post Doc at the surface science group of the physics department. Since 2016, he has been working as a scientist and product manager for electrical analysis systems in SEM and TEM at point electronic GmbH.

Tues
15:40 - 16:00

Advancing the Quantification Workflow for 2D Charge Carrier Profiling by Scanning Spreading Resistance Microscopy

Thomas Adlmaier I Infineon Technologies Dresden GmbH I Germany

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Session C: Novel FA Techniques

SSRM (Scanning Spreading Resistance Microscopy) is an established technique for 2D dopant visualization with high lateral resolution (~1-10nm) and sensitivity (~1E14-1E20 1/cm^3). While normal SSRM produces qualitative information about doping shapes and sizes, quantitative SSRM adds a calibration measurement on a known dopant reference to extract absolute values on top. While this approach seems easy in theory, in actual practice one is met with numerous complications, often leading to a long and costly analysis. To alleviate such complications, we introduce two innovations: Firstly, we propose a novel Partial-Staircase (PSC) dopant reference profile which combines the advantages of the conventional staircase profiles and sole reference implants into one. Secondly an extended sample preparation workflow is presented, which brings area of interest and dopant reference into high proximity and enforces the exact same measurement conditions on both by design. Put together, both innovations reduce analysis complexity while increasing quantification accuracy.

Thomas Adlmaier works at Infineon Technologies Dresden GmbH as a Failure Analysis Engineer in the SPM Team since 2021. Currently he is pursuing his PhD in the same field focusing on the quantification of Scanning Spreading Resistance Microscopy (SSRM). Before that Thomas graduated with a Master of Science in physics at the University of Technology Dresden, writing on the quantification of Scanning Capacitance Microscopy (SCM) in his graduation thesis.

Tues
16:00 - 16:20

FA methodologies for silicon photonics devices

MR Sharmal IMEC and KU Leuven I Belgium

Anjanashree.MankalaRamakrishnaSharma@imec.be

Session C: Novel FA Techniques

Photonic integrated circuits (PICs) developed on silicon photonics (SiPh) platforms are a significant breakthrough in the field of data communication as they increase the speed and capacity of data transmission with lesser power consumption. It integrates devices such as lasers, photodetectors, optical waveguides, and modulators on the silicon substrate and can be fabricated using an industry-standard CMOS process. This has pushed SiPh devices into the commercial manufacturing phase. Hence, it is very relevant to perform the failure analysis (FA) to ensure the reliability of these devices.
In my presentation, I will discuss the FA methodologies used for defect localization in emerging devices used in PICs such as photodetectors and laser diodes, fabricated at imec. In particular, germanium photodetectors and InGaAs/GaAs nano-ridge p-i-n diodes which are extensively researched and have the potential to be adapted in the industry, are used as test devices for this study. The application of conventional and advanced FA techniques such as lock-in thermography (LIT), thermoreflectance, and electron beam-based nanoprobing based on their spatial resolution will be discussed.

Anjanashree MR Sharma is a PhD student at the Department of Materials Engineering, KU Leuven and IMEC in Belgium. She is working on the development of failure analysis techniques for advanced semiconductor devices, under the supervision of Prof. Ingrid De Wolf. She completed her master's degree in nanoscience and nanotechnology from KU Leuven in 2021. Her PhD research focuses on improving lock-in thermography (LIT) technique for defect localization in emerging semiconductor devices.

Tues 17:00 - 18:00	**Panel Discussion:** **Failure Analysis roadmap status & vendor feedback**	Session D: Panel Discussion

The FA Technology Roadmap initiative, which is driven by ASM's Electronic Device Failure Analysis Society (EDFAS) Society, is actively involved to identify the longer term needs and gaps of failure analysis methods and equipment related to new trends in semiconductor device manufacturing. The purpose of the FA Technology Roadmap is to leverage the technical expertise captured throughout the industry to identify both current and future FA challenges and to serve as an international technical platform for failure analysis. The goal is to bridge existing and upcoming gaps by leveraging both the expertise of equipment providers and the research conducted in academic labs.

Last year, during the panel discussion, the invited panelists provided a summary of the progress made in the FA Technology Roadmap activities. They highlighted the ongoing efforts to identify and analyze the current and future FA challenges. This involved conducting an industry-wide gap analysis, which helped in mapping out the areas that require further attention and improvement.

This year, the focus is on the vendor's responses to the industry-wide gap analysis survey. The committee is actively seeking input and feedback from equipment providers to gain insights into their perspectives on the identified gaps. This will enable the committee to gather valuable information on potential solutions and innovations that can address the challenges faced by the industry.

The FA Technology Roadmap Committee recognizes the importance of collaboration and knowledge-sharing between equipment providers, academic labs, and other stakeholders in the FA industry. By working together, they aim to drive advancements and improvements in FA techniques, tools and workflows.

Keith Serrels I NXP Semiconductors I US
Libror Strakoš I Thermo Fisher Scienitfic I Czech Republic
Chris Richardson I Allied High Tech Products, Inc. I US
Martin Igarashi I TeraView LTD I UK
Lukáš Hladík I TESCAN GROUP, a.s. I CZ
Wenbing Yun I Sigray, Inc. I US
Thomas Rodgers I Carl Zeiss Research Microscopy GmbH I DE
Peter Hoffrogge I PVA TePla Analytical Systems GmbH I DE

Wed 08:00 - 09:00	**Tutorial: Machine Learning Based Data and Signal Analysis Methods for the Application in Failure Analysis**	Session E: Tutorial

Michael Kögel I Fraunhofer IMWS I Germany

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Since its release, ChatGPT has sparked ongoing fascination for its human-like responses, reflecting the growing interest in AI's potential applications across various fields. In microelectronics failure analysis, a discipline aiming for reliability and performance improvement, machine learning holds promise by aiding defect localization and subsequent analysis through destructive inspection tools. The ability to process large datasets and extract correlated information benefits defect analysis, assisting in identifying root causes.

This tutorial introduces machine learning and deep learning to failure analysts covering historical context, data handling, feature extraction, learning algorithms, model evaluation, and optimization. It explores convolutional neural networks for image processing and advanced neural network applications like auto-encoders and natural language processing. Case studies demonstrate ML's potential in failure analysis, such as bill of material generation from optical images, automatic defect detection on PCBs, void segmentation in x-ray images, and SEM image denoising.

Michael Kögel graduated in 2015 from Leipzig with a Master of Science in Electrical Engineering and Information Technology. Since then, he has worked as an engineer specializing in failure analysis of semiconductor components at IMWS-CAM. He is a member of the team focusing on non-destructive defect localization in the field of failure analysis and metrology in microelectronics. His experience encompasses application and development of techniques such as Signal Processing, Scanning Acoustic Microscopy, Lock-In Thermography, and Magnetic Current Imaging.

Wed 09:40 - 10:20	**Keynote:** **SiC power devices and related robustness and reliability aspects**	Session F: SiC and GaN power electronics

Peter Friedrichs I Infineon Technologies AG I Germany

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The implementation of wide band gap based power semiconductor solutions, was growing substantially during the last years, Driving forces behind this market development are global megatrends like energy saving, de-carbonization and effective use of scarce resources. One of the success factors of implementing SiC as a power device material is the chance to adopt many of the well-known device concepts and processing technologies from silicon.

Thus, many of the procedures used to verify the long-term stability of silicon devices could be transferred to SiC. Nevertheless, a deeper analysis has shown that SiC based devices require some additional and different reliability tests compared to Si based devices. Aspects like anisotropic material properties, higher electric fields or faster transients may have an influence on nearly all established qualification tests.

Furthermore, for many existing qualification standards that specify accelerated tests, models are used to extrapolate the test data and correlate it to real world application conditions. These model parameters need to be verified for their application and accuracy with respect to SiC. The keynote presentation will give a more detailed inside into the current status of SiC related reliability assurance procedures, also addressing ruggedness aspects.

Dr. Peter Friedrichs received his Dipl.-Ing. in microelectronics from the Technical University of Bratislava in 1993 and finished his Ph.D thesis at the Fraunhofer Institute FhG-IIS-B in Erlangen. His focus area of expertise was the physics of the MOS interface in SiC. In 1996 he joined the Siemens AG and was involved in the development of power devices on SiC. Peter joined SiCED GmbH & Co. KG, a company being a joint venture of Siemens and Infineon, on March the 1st, 2000. Since July 2004 he was the managing director of SiCED. In 2009 he achieved the Dipl.-Wirt.-Ing. From the University of Hagen. After the integration of SiCED's activities into Infineon he joined Infineon Technologies AG on April 1st, 2011 and acts currently as Fellow SiC Innovation.

Wed 10:40 - 11:00	**Gate-switching instability in silicon carbide power MOSFET's**	Session F: SiC and GaN power electronics

Dick Scholten I Robert Bosch GmbH I Germany

Threshold voltage drift in MOSFET's due to prolonged application of a high constant gate voltage at high temperature is a well-known degradation mechanism and has been observed in MOSFET-technologies based on silicon, gallium nitride, or silicon carbide. A peculiarity of silicon carbide MOSFET's is that high numbers of bipolar gate switching events result in a threshold voltage drift that exceeds the drift expected from constant voltage stress alone. The presentation will detail the properties of this degradation mechanism and will give an overview of possible root causes currently under discussion. Arguments to test worst case scenarios on chip level rather than on module level will be discussed.

Dick Scholten received his degree in experimental physics from the University of Groningen in the Netherlands (1998) and his Ph.D. degree in physics from the University Erlangen-Nürnberg in Germany (2002).

He has been a visiting research fellow at the Instituto di Fysica Nucleare in Pisa in Italy, where he worked on gamma ray detectors. In 2003 he joined his current employer, Robert Bosch GmbH, initially as a researcher in the field of MEMS and sensor devices. Since 2008, he is working on wide bandgap power transistors with focus on silicon carbide MOSFETs.

Wed 11:00 - 11:20	**Integration of free-standing single crystal diamond (SCD) nanomembranes in ultra-wide bandgap electronics**	Session F: SiC and GaN power electronics

Andreas Graff I Fraunhofer IMWS I Germany

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Single crystal diamond (SCD) has great potential for next-generation RF and power electronics, because of the excellent thermal conductivity and high carrier mobility. Toward the realization of high-performance ultra-wide bandgap (UWBG) electronics, it is crucial to create p-n junctions by complementing p-type property of SCD with n-type property of other UWBG. Free-standing SCD nanomembranes (NMs), enables us to heterogeneously integrate SCD with other UWBG semiconductors via a semiconductor bonding technology. SCD NMs technology and hetero-integration technology will be discussed covering the fabrication process and material properties of SCD NMs, as well as the device manufacturing process and electrical property of SCD NM / Ga2O3 heterojunction p-n diodes. Doped and undoped SCD epitaxy layers were deposited on (001) SCD wafers. Hydrogen implantation was performed to separate the structured top portion of the SCD which then becomes NMs after a post annealing process. The released SCD NMs were transferred to n-/n+ Ga2O3 epitaxy wafer via a micro-transfer printing process to create SCD NM/ Ga2O3 heterojunction p-n diodes. The device exhibited excellent electrical properties. The breakdown electrical field was measured to exceed 2MV/cm at room temperature, demonstrating the superior performance of the UWBG p-n heterojunction diode based on SCD NM technology.

Andreas Graff studied physics at the RWTH Aachen Germany and did his Ph. D. at the Max-Planck-Institute for Microstructure Physics in Halle, Germany, in the field of solid state reactions investigated by electron microscopy. He is scientific staff member at the Fraunhofer Institute for Microstructure of Materials and Systems IMWS in Halle, Germany since 2003. He is working on physical failure analysis of semiconductor devices especially with electron microscopy techniques. Special interest are new semiconductor materials and electron spectroscopy.

Wed 11:20 - 11:40	**Power devices Failure Analysis Use Cases Using High voltage OBIRCh workflows**	Session F: SiC and GaN power electronics

Antoine Reverdy I Sector Technologies I France

antoine.reverdy@sector-technologies.com

Nowadays, electrification trends, especially in the automotive market, are driving the need for high power electronics. In the past years, Silicon Carbide (SiC) and Gallium Nitride (GaN) microelectronics solutions have been introduced on the market as they have clear benefits for such application (its key benefits include delivering higher voltage operation, wider temperature ranges and increased switching frequencies). These Wide Band Gap (WBG) technologies are relatively new, thus, quality control and reliability understanding are critical topics to make sure they will remain sustainable.

We will present 3 Failure Analysis use cases and workflows related to power device technologies. In collaboration with our Fault Isolation tool equipment supplier (ThermoFisher Scientific), we have developed a High Voltage solution to address HV-O.B.I.R.Ch. and HV-Photoemission analysis on our Meridian S Platform. This solution allows addressing our current High Power devices roadmap up to 3kV.

Antoine Reverdy received his Master in microelectronics and an engineering degree in Digital Microelectronics in 2006 from the Superior National School of Electrotechnics, Electronics, computing science, Hydraulic and telecommunication (ENSEEIHT) in Toulouse. In 2008, he received his PhD on Failure Analysis for advanced technologies with a specific focus on laser based techniques (OBIRCh, DLS, lock in OBIRCh). Since 2009 he is working for Sector Technologies as an application engineer specialist on fault isolation techniques such as emission microscopy, laser based techniques (OBICRh, DLS, LVx), lock in thermography, EOTPR.

Wed
13:00 -13:40

Keynote:
Applied Microstructure for AI: From Electrons to Devices & From Diagnostics to Informatics

Session G:
Failure analysis workflows and digitalization

Prof. Dr. Zhiheng Huang I Sun Yat-sen University I China

hzh29@mail.sysu.edu.cn

Although not even mentioned in the original launch of the US materials genome initiative (MGI) in 2011, AI has now been identified the true enabler and driving force of MGI.Latest progress reports Google DeepMind and robots joined forces to discover and synthesis new materials. Microstructure of materials should be treated as a system as perceived by the pioneering work of C.S. Smith. Highlighting the achievements of MGI in the past decade, it is the atomic scale details represented by DFT-based calculations and graph neural network that have attracted most of the interests. Phase spaces that reflect elemental combinations to yield desirable chemistry or physics have been explored, but the results that AI recommends still deserve better interpretations. Based on a convergence amongst deep neural networks, wavelets, and physiology of human brain, and the theory of Mallat Scattering Transform, this talk introduces the principles behind the recent proposed Microstructure Hierarchy Descriptor (μSHD). The μSHDs are designable and reduced order indices that can be used to establish quantitative linkages between structures, properties, and failure analyses. Applied microstructure diagnostics spanning structures from electron to device levels, and failure analyses on 3D and power electronics will be discussed with a vision from μSHD data to microstructure informatics and AI.

Zhiheng Huang received the B.Eng. & M.Eng. degrees from Harbin Institute of Technology (China), and the Ph.D. degree from Loughborough University (UK). He did postdoctoral research at Loughborough Uni. and Max Planck Institute for Iron Research (MPIE, Germany). In June 2008, he joined Sun Yat-sen University, where he is currently an Associate Professor in the School of Materials Science & Engineering. He successfully completed the project on Integrated Computational Materials Engineering for 3D Electronic Packaging funded by the Guangzhou Pear River Sci. & Tech. Nova program, along with his NSFC funded early career project. In a recent NSFC funded key project on oxidation and corrosion of SiC-based ceramics at high temperatures, he proposed the MicroStructure hierarchy Descriptor (μSHD) and utilized it as a tool to quantify the microstructure of sintered SiC ceramics and establish the linkages between μSHDs and material properties. Recent years have seen his active participation in the field of Materials Genome Engineering and practice of μSHDs for metals, polymers, physical and failure analysis, and food science.

Wed
13:40- 14:00

An Artificial Intelligence Powered Reconstruction and Metrology Workflow for Semiconductor Packaging Development using High-Resolution 3D X-ray Microscopy

Session G:
Failure analysis workflows and digitalization

Allen Gu I Carl Zeiss Research Microscopy Solutions I USA

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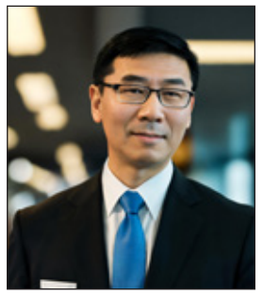
Over the past decade, the innovations in semiconductor packaging have been the catalyst to improve electronics device performance. Among many rapidly emerged package architectures, 3D multi-chip stacking and heterogenous integration become particularly attractive for the capabilities to increase I/O density, save power consumption and shorten the time to market. However, the IC packaging industry faces the challenge to find an effective inspection and metrology solution for these innovative packages. 3D X-ray microscopy (XRM) technique has been rapidly and widely adopted to failure analysis labs in semiconductor community. With its non-destructive and high resolution imaging capabilities, deeply buried defects can be visualized and analyzed prior to physical cross-section. In this paper, we propose a novel imaging and quantification workflow to enable 3D structural measurements using the 3D XRM imaging technique. The test vehicle was a multi-die coupon with 15-layer stacks for each die. The fabrication process started with the IMEC's flip chip fan-out wafer level packaging (FO-WLP) process flow to connect a thin Si bridge to the logic die substrate. A standard thermal compression bonding (TCB) process was followed to complete the delicate die attachment. To validate the die placement accuracy and bond line thickness uniformity, a measurement workflow is required to evaluate and optimize bonding quality and process flow.



Dr. Allen Gu is a senior sector manager of ZEISS Microscopy in developing microscopic solutions for next-generation semiconductor packaging. With a background in materials science and engineering, he's spent his past 18 years in a variety of microscopy technologies with focus on micro/nanoscale imaging and analysis. He joined Carl Zeiss X-ray Microscopy in 2010 and played a leading role in pioneering X-ray imaging techniques for semiconductor failure analysis. Now the ZEISS XRM becomes the world's most advanced 3D X-ray microscopy brand among non-destructive techniques. Prior to his ZEISS career, he severed as a Sr. applications scientist for several microscopic technologies in Pacific Nano and Agilent, USA. He has (co)authored about 70 journal articles, conference paper, presentations, and US patents.

Wed 14:00- 14:20	**ML assisted defect detection for reliable failure analysis in microelectronic components**	Session G: Failure analysis workflows and digitalization

Amit Kumar Choudhary I Matworks GmbH I Germany

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Microelectronic products from the semiconductor industry are crucial for many recent technological advances in automotive industries and intelligent production systems but have reliability issues that require failure analysis to investigate the failures' root cause. Using visual inspection systems such as cameras or microscopes, images of microelectronic products or components are acquired to be evaluated for potential defects and anomalies arising from the manufacturing process. Manual evaluation of such a large amount of data carries the risk of subjective errors, consumes lot of time and efforts, leading to backlogs that can drive costs.

In this work, we developed defect detection models using advanced machine learning and computer vision approaches that are more reliable, with detection accuracy close to or sometimes better than manual or existing approaches. The developed models for different use-cases (voids, phases, anomalies), have an accuracy ranging from 86 % to 94 % and has advantage of being time-efficient by a factor of 20x to 30x for different tasks. Each use-case involves image data from various microscopy techniques such as OM, SEM, X-ray and SAM.

Amit Kumar Choudhary is currently working as a Software Engineer at Matworks GmbH and has experience in developing business-specific solutions related to automated microscopy using machine learning and computer vision techniques.

Wed 14:20 - 14:40	**In Depth Logic Analysis on Digital Designs**	Session G: Failure analysis workflows and digitalization

Fabian Rudau I Robert Bosch GmbH I Germany

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Physical failure analysis (physical FA) for automotive devices requires an efficient FA workflow to satisfy the customer's expectations of on-time-delivery and success rate. Field return complaints typically contain only one single failing device. Hence, every step in fault isolation and physical preparation requires a high confidence level in order to avoid the risk of losing the failure in subsequent destructive steps.

We will present a software to support the FA engineer to quickly identify correct and incorrect logic signals in digital circuits enabling fast and successful FA.

After studying physics with a focus on solid-state physics, followed by a PhD at the University of Tübingen, Fabian Rudau has been working at BOSCH in Reutlingen for about six years in the field of ASIC failure analysis. His main activities are related to electrical characterization and optical localization techniques like OBIRCH, PEM and LVP.

Wed 14:40- 15:00	**Integrated Workflows for Failure Analysis**	Session G: Failure analysis workflows and digitalization

Christian Hollerith I Infineon AG I Germany

christian.hollerith@infineon.com

In EU-funding project FA4.0, the idea of Integrated Workflows within FA has been defined and is being developed. Integrated Workflows in FA means that sample remains on the same sample holder in a whole workflow and data, especially position data of regions of interest, es being transported from tool to tool to simplify the workflows for the user as well as increase efficiency. To enable these workflows on tools of different vendors, exchange formats for data as well as a common universal sample holder has to be defined which is established also as industrial standard. This presentation will show an example how this principle can work including a TePLA-SAM and a Tescan-PFIB and also of the necessary standardization process in cooperation with SEMI.

Dr. Christian Hollerith is Principal Engineer in the Failure Analysis department of Infineon in Munich with expertise in the fields of Nanoprobing, SEM, SAM and Application of AI. He studied physics at TU Munich from 1996 to 2001. He did his diploma and PhD thesis about the application of transition edge sensors for EDS until 2006. Subsequently, he joined FA lab Munich of Infineon as part of the FA-team for communication products. At this position he was involved in developments in various fields of FA. He worked within several EU funding projects like SAM^3, FA4.0 and now FA^{2}IR.

Wed 15:00 - 15:20	**In-situ AFM-in-(FIB)SEM workflow for site-specific & correlative failure analysis of semiconductors**	Session G: Failure analysis workflows and digitalization

Libor Strakoš I Thermo Fisher Scienitfic I Czech Republic

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The AFM-in-SEM approach combines Atomic Force Microscopy (AFM)-based techniques with Scanning Electron Microscopy (SEM)-based or Focused Ion Beam FIB-SEM based techniques. It provides a means to integrated correlative approach for studying semiconductor materials and devices. This solution allows for the non-destructive mapping of diverse electrical properties of trenches, measuring gate dimensions or localizing defects, which could help to understand the device processes. This approach provides the advantages of combining the benefits of capabilities of site-specific sample preparation by FIB, ultra high-resolution imaging by SEM and AFM techniques. The integration offers additional benefits, including measuring properties at the exact location under in-situ conditions and avoiding sample or environmental changes such as differential pressure or sample contamination. Typical example of such site specific analysis is dopant concentration profiling on the level of individual device

Libor Strakoš holds a degree in Electrical Engineering from Brno University of Technology and has multi-year applications experience developing charged particle microscopes for failure analysis of semiconductors with focus on TEM sample preparation and diffraction techniques in SEM.

Wed 15:20- 15:40	**Automated SEM/EBIC Workflow for Wafer Level Failure Analysis**	**Session G: Failure analysis workflows and digitalization**

Oscar Recalde I Kleindiek Nanotechnik GmbH I Germany

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In semiconductor electronics, efficient failure analysis is crucial for reliability. Here, we present an automated workflow for precise and rapid failure analysis. Optimizing probe placement significantly cuts analysis time while improving result reliability, which is particularly beneficial for beginner nanoprobing users.
In a proof-of-concept experiment, the probe alignment and landing process was successfully achieved through a few clicks. Our study demonstrates that this process can be successfully executed not only at high electron beam energy voltages but also at low electron beam voltages, ensuring versatility and robustness in failure analysis workflows.
Furthermore, our study introduces a semi-automated failure analysis workflow incorporating encoded micromanipulators for examining devices down to 3 nm. All this, coupled with advanced data processing integrated into the Kleindiek Advanced Probing Tool software and Electron Beam Induced Current (EBIC) analysis, enables comprehensive characterization of device failures. An automated workflow signifies a significant advancement in semiconductor failure analysis for improved reliability and innovation.

As a new engineer at Kleindiek Nanotechnik, I merged material science and electron microscopy expertise acquired through a Ph.D. at TU Darmstadt. My focus lies in in situ operando techniques for transmission electron microscopy in oxide-based electronic devices. I specialize in elemental analysis and MEMS device integration, proficient in focus ion beam systems, SEM, and advanced TEM methods. Eager to innovate, I'm committed to supporting Kleindiek Nanotechnik's precision engineering mission in the semiconductor industry.

6 Exhibition

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INFRATEC GMBH

InfraTec Infrarotsensorik und Messtechnik GmbH, founded in 1991, has its headquarters in Dresden, Germany and employs about 240 people. With its own design, manufacturing and distribution capabilities InfraTec is one of the leading suppliers of commercial thermal imaging technology including turnkey thermographic automation solutions.
E-LIT – Lock-In Thermography for Electronics – is a modular automated test bench for analysing electronic & semiconductor components and is equipped with high-performance thermographic cameras. It allows non-contact failure analysis and detects e.g. inhomogeneous temperature distribution, leakage currents, cold joints, latch-up effects and soldering issues.

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MUEGGE GMBH

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EUROFINS MASER B.V.

Eurofins MASER is an independent engineering service company. Since 1993 we have offered Reliability Test and Failure Analysis Services to the semiconductor and electronic systems industry. We offer a wide range of qualification procedures (AEC Q100/JEDEC/MIL/IEC) to qualify the products according to the latest international standards or to your specific requirements. Whether a company is active as Fabless Semiconductor Manufacturer, IC Design House, Electronic Manufacturing Service (EMS) Provider or Original Equipment Manufacturer (OEM) we can support them with their daily Reliability Test or Failure Analysis challenges.

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PVA TEPLA ANALYTICAL SYSTEMS GMBH

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POINT ELECTRONIC GMBH + IMINA TECHNOLOGIES S.A.

point electronic GmbH is a supplier of detectors, acquisition and control systems for SEM, TEM and Micro-analysers. The company is a leader in developing solutions for e.g. Topography, EBIC, EBAC/RCI and Electrical Failure Analysis. It provides microscope services, up to complete electronics and software upgrades.

Imina Technologies SA is a Swiss manufacturer of robotic solutions for the characterization of samples under optical microscopes, FA inspection tools, Probe Stations and scanning electron microscopes (SEM/FIB). Imina is one of the leaders in the semiconductor test equipment market for micro & nanoprobing and electrical failure analysis.

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HAMAMATSU PHOTONICS DEUTSCHLAND GMBH

Hamamatsu Photonics is one of a few companies in the world that develops a wide range of light sensors, such as photodiodes, image sensors and photomultiplier tubes, as well as number of light sources.
Our portfolio of more than 10,000 products does not only include components, but also fully integrated systems, like our emission microscope PHEMOS X for failure localization in semiconductor devices.
The Phemos X is designed for the analysis of Logic and Power Devices, including advanced CMOS technologies. It can be equipped with up to 5 lasers from VIS to NIR and different detectors. Its structure is flexible to use any of these techniques, either individually or as „all in one".

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JP KUMMER SEMICONDUCTOR TECHNOLOGY GMBH

The JP Kummer Semiconductor Technology GmbH is a specialist European Distributor of instruments and consumables mainly for the Semiconductor industry, but also for the Medical Device, Aerospace, Solar and related Industries. We attach great importance to trade with reliable products. We verify the quality of the manufacture of the products sold by us regularly. Our employees are trained in continuous intervals of our suppliers and maintain them with an intensive exchange of information.
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Website::	www.jpkummer.com
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ALLIED HIGH TECH PRODUCTS, INC

For over 40 years, Allied High Tech Products has provided sample preparation products for failure analysis to the microelectronics industry. Allied manufactures cutting-edge equipment at its facilities with all design, manufacturing and assembly taking place in-house to ensure the highest quality equipment is produced. Allied's state-of-the-art equipment includes the X-Prep® Precision Polishing/Grinding/Milling Machine, MultiPrep Polishing System, MetPrep Grinding/Polishing Systems and TechCut Sectioning Saws. Please stop by Stand #14 for more in-depth information.

Address:	Carmenita Road 16207 90703 Cerritos I USA
Website::	www.alliedhightech.com
Phone:	+1 3106352466
Email:	info@alliedhightech.com

Geneal Information

Registration On-Site

You can pick-up your name badges:
Tues, 4th June 2024 I 08:00 - 17:40
Wed, 5th June 2024 I 07:30 - 13:00

Proceedings

Proceedings can be downloaded. A download link and password will be emailed to all registered participants after the workshop.

Workshop Language

The official language of all presentations is English.

Website

For further information, please visit:
www.cam-workshop.de

Airport

Leipzig-Halle Airport is only 15 minutes away from the city center by train.
Take the city train line S5 or S5x from the airport to Halle main station.

Parking

There are two dedicated parking areas near the venue free of charge.

Train

The city train lines S5 and S5X offer a direct connection between Halle main station and Leipzig airport.
Form the main statiion, you can take the tram (numbers 4 or 5) to the stop "Weinberg Campus". Alternatively take a taxi to Leibniz IAMO, Theodor-Lieser-Strasse 2, Halle.

Taxi

Taxis can be called:
Halle Taxi + 49 345 525252 / 212121
Taxi Kobsch +49 345 5606222

Tram

Trams lines 4 & 5 connect the workshop venue (stop: "Weinberg Campus") to the city center and the main station.

Conference Venue

Leibniz IAMO I Theodor-Lieser-Strasse 2 I 06120 Halle

Social Program

Tuesday, 4th June 2024 | 18:00 - 19:00 | Exhibition Area

Drinks Reception
Be sure not to miss our drinks reception in the exhibition area – starting straight after the workshop on Tuesday, 25th April 2023.
Refreshments and finger foods will be provided for all delegates attending the conference.

Venue: Leibniz IAMO I Theodor-Lieser-Straße 2 I 06120 Halle (Saale)

Tuesday, 4th June 2024 | 19:00 - 22:00 | Gardens at Leibniz IAMO

Networking Dinner
Our live band will be performing popular classics while you enjoy a picnic in the beautiful gardens of Leibniz IAMO. This gives you a chance to continue your discussions about FA trends, developments and products within a relaxed and informal atmosphere. All participants are invited to join us!

All participants and exhibitors are invited to join us!

Venue: Leibniz IAMO I Theodor-Lieser-Straße 2 I 06120 Halle (Saale)

We would like to thank our sponsors and partners for their support.

Fraunhofer IMWS

hallesaale HÄNDELSTADT

Save the Date

for the 12th CAM-Workshop

20th and 21st May 2025

Innovation in Failure Analysis and Material Diagnostics of Electronics Components

Industry Workshop and Technology Exhibition

Halle (Saale) I Germany

Tuesday, 04th June 2024

08:00 - 09:00	Registration	Lobby
09:00 - 10:40	Introduction and Keynotes	Lecture Hall
10:40 - 11:20	Coffee Break I Exhibition	Lobby
11:20 - 13:20	Heterogeneous Integration	Lecture Hall
13:20 - 14:40	Lunch Break I Exhibition	Lobby
14:40 - 16:20	Novel Failure Analysis Techniques	Lecture Hall
16:20 - 17:00	Coffee Break I Exhibition	Lobby
17:00 - 18:00	Panel Discussion	Lecture Hall
18:00- 19:00	Drinks Reception I Exhibition	Lobby
19:00 - 22:00	Networking Dinner	Gardens

Wednesday, 05th June 2024

07:30 - 09:40	Registration	Lobby
08:00 - 09:00	Tutorial	Lecture Hall
09:00 - 09:40	Coffee Break I Exhibition	Lobby
09:40 - 11:40	Wide Band Gap Power Electronics	Lecture Hall
11:40 - 13:00	Lunch Break I Exhibition	Lobby
13:00 - 15:40	Failure Analysis Workflows and Digitalization	Lecture Hall